Ultra Low-Latency UDP FPGA IP For 10 &25 Gbit/s Ethernet

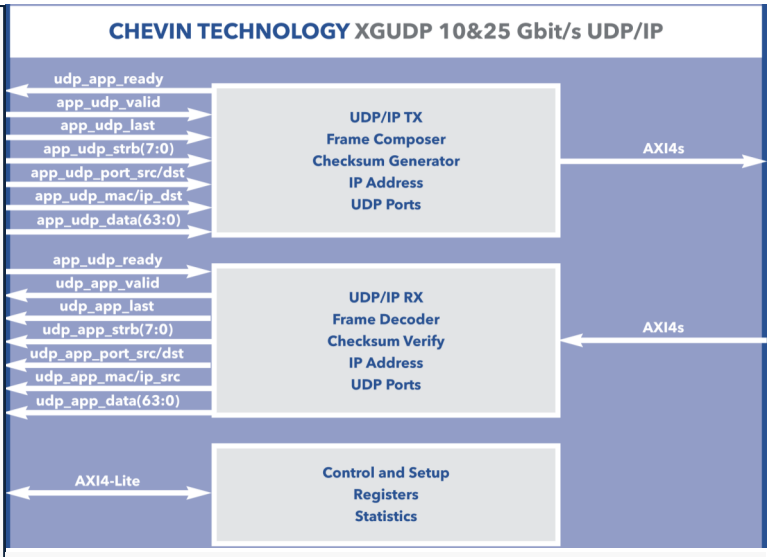
CT1012-XGUDP - Product Brief - Version 1.8 – 3rd July 2017

Chevin Technology's 10G & 25G UDP Ethernet IP is FPGA Synthesisable EndPoint with Checksum Offload for ultra low-latency connectivity. The 10G & 25G UDP IP cores simplify FPGA integration of an ultra fast UDP/IP layer in any FPGA by handling the complete Ethernet frame assembly.

The XGUDP offloads frame assembly with hardware accelerated checksum calculation for UDP datagrams. The XGUDP is a RTL block that can be used directly with any MAC that supports a 64bit data interface with byte lane enables. The application side FIFO provides independent TX/RX buffering and flow control between Application logic and UDP, over a streaming interface 64bit interface in a single clock domain. Remote port information is multiplexed with the streaming interface to provide a flexible solution for application logic. A detailed statistics block provides a running count of frames sent and received, number of bytes sent/received, frames dropped due to flow control, last sent/received frame size and optional timestamp. Reference designs are available on selected boards using standard software development tools when integrated with higher layers from Chevin Technology's range of IP blocks.

Key Features

- AXI4s MAC & Application Interfaces
- Designed to UDP specification RFC 768
- Compose/Decompose complete UDP Datagrams
- IP frame Checksum Generator/Checker
- Jumbo frame support up to 32k
- Configurable operation port filtering
- 1-64k Ports (configurable ports & filters)
- Detailed traffic analysis statistics collection
- Integrated Streaming FIFO – 4 Block RAMs
- Integrated IP Checksum Generator/Check
- Flow Control between MAC/User logic
- Consistently low and predictable latency with zero frame jitter



Deliverables

- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Designs for Xilinx KC705 board & AlphaData boards ADM-PCIE-KU3, ADM-PCIE-8V3, ADM-PCIE-9V3,
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA

Latency Figures

TX 38.4 ns, RX 38.4 ns

Round trip delay MAC -> APP -> MAC 102.4ns

(Figures above include 33.6ns of inherent protocol latency)

FPGA Resource Figures

Devices: Virtex UltraScale: 2480 LUTs

Kintex Ultrascale: 2480 LUTs , Kintex-7: 3088 LUTs

Small Memory Footprint 14 RAMs

Options: + ARP/ICMP 920 LUTS

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10 & 25Gbit/s Ethernet UDP

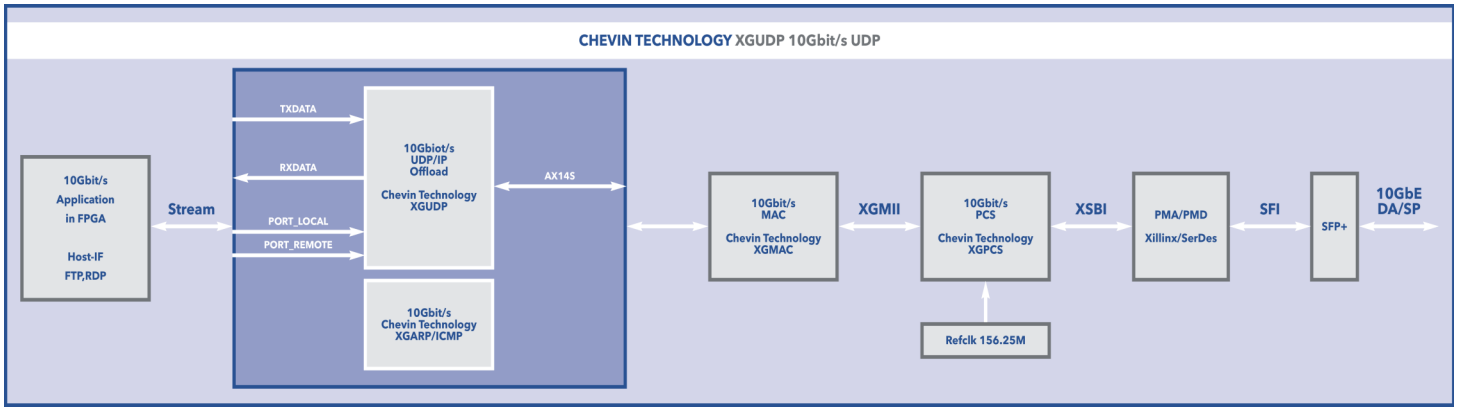
XGUDP - Integration in FPGA

A simple host interface allows control and configuration of the XGUDP blocks' registers and statistics.

The reference design can be used to speed up integration work with the help of a UART host interface port and example software and build scripts and constraints. The UDP send/receive port number can be specified as an input to the UDP block or a control and status register to allow send/receive to any number of UDP ports.
All logic is clocked in a single clock domain @156.25MHz.

The application side can connect directly to any 64bit MAC with an easy to use streaming AXI4s interface.
We recommend pairing the XGUDP with Chevin Technology's XGMAC, an ultra-low-latency Ethernet MAC and other stack layers such as TCP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.

The XGARP/ICMP block adds RTL-hardened functions for ICMP and ARP to any FPGA application. The all-RTL block includes part of the ARP protocol which is used to discover nodes on a network and to automatically associate MAC/IP addresses. The ICMP protocol supports simple messages such echo request and reply. ICMP is used to "ping" the FPGA on a network. A lean FPGA application can be built with the two protocols as a minimum to provide discovery of the FPGA node and low level communications.
Using the XGARP/ICMP block not only simplifies integration by avoiding the use of a CPU it also provides a very rapid response time of sub-100ns to both ARP and ping requests.



Chevin Technology IP

10G Ethernet

10G PCS/PMA

10G LL MAC & PCS/PMA

SSD STORAGE

SATAv3.2 – 1.5/3/6Gbit/s SSD Host Ctrl

25G Ethernet

25G MAC

25G PCS/PMA

25G LLMAC & PCS/PMA

ETHERNET PROTOCOLS

25G TCP
XGTCP - 10Gbit/s TCP Server/Client
XGICMP/ARP – 10Gbit/s support library
XGUDT4 – 10Gbit/s UDT4 Server

Markets

- Finance
- Telecoms
- Broadcast
- Defense/ Government
- Oil and Gas

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining

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