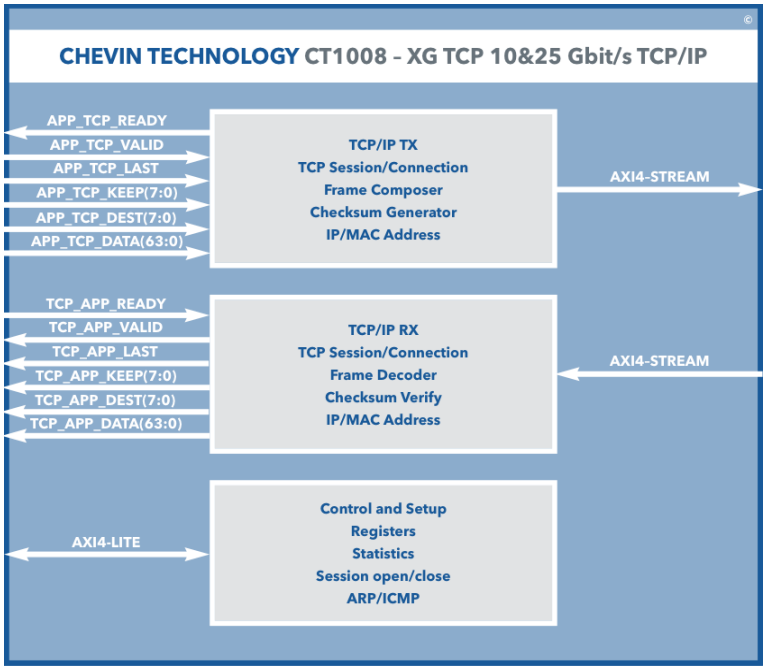
TCP/ Internet Protocol for 10 &25 Gbit/s Ethernet

CT1008-XGTCP - Product Brief - Version 1.1 – 7th February 2019

The TCP/IP (Transmission Control Protocol/ Internet Protocol) is an Ethernet IP core for FPGAs that incorporates both the transport and internet layer protocols to deliver reliable, end to end network communications using the internet or on private networks. Chevin Technology's TCP/IP Offload Engine is an FPGA Synthesisable Ethernet TCP/IP server/client in a lean and fast , all-RTL solution.

The TCP IP core can be used with both 10G & 25G Ethernet IP cores for reliable, low-latency connectivity in any FPGA using a minimum of resources. Chevin Technology's TCP IP core offloads the TCP protocol using fast and efficient logic for checksum calculation, and is easily integrated alongside other protocols to provide an easy path for the development of TCP enabled FPGA applications.



Key Features

- *Low gate count*
- *1 to 256 simultaneous TCP/IP sessions*
- *Server/Client, configurable per session*
- *Low latency, high throughput performance*
- *Programmable per session receive/congestion window*
- *Internal/external memory*
- *Configurable TX & RX buffer size: 1KB-1GB*
- *64-bit AXI4 stream @ 156.25 MHz*

Throughput & Latency Figures

TCP send/receive rate: 9.5 Gbps (1.2 GB/s)

TX / RX– Latency < 1 us

FPGA Resource Figures

Devices: Xilinx Virtex UltraScale; Kintex Ultrascale; Kintex-7; Zynq

Small Memory Footprint 25 BRAMs + packet buffer;

12000 LUTs for 16 sessions

Options: External DDR3 packet buffer;

+ ARP/ICMP 1100 LUTS

Deliverables

- Encrypted compiled netlist
- Datasheet & User Guide
- Reference Designs
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA

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TCP/IP for 10 & 25Gbit/s Ethernet

TCP/IP - Integration in FPGA

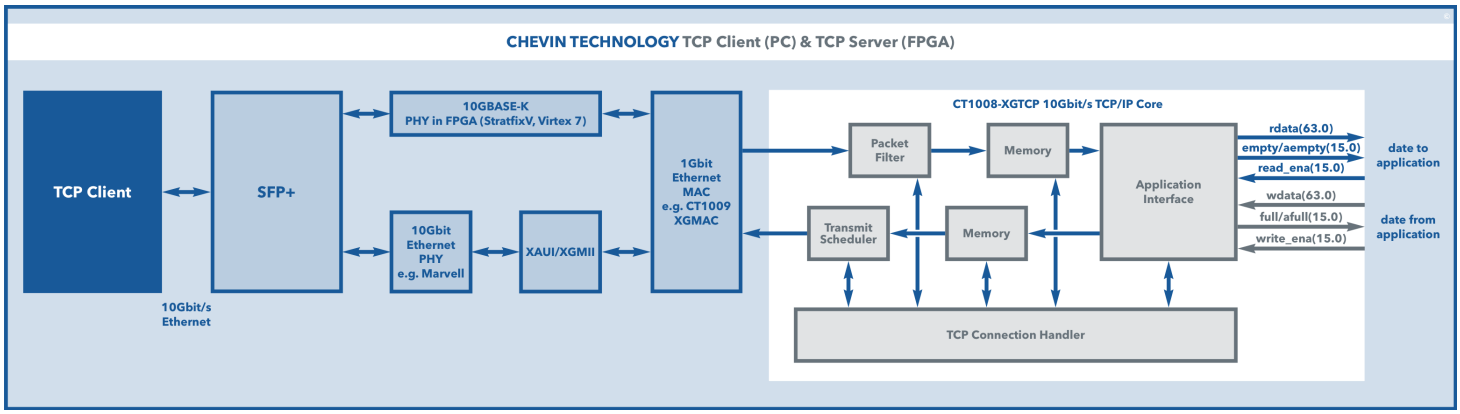
The TCP/IP Offload Engine provides a quick path to creating TCP enabled applications with a minimum of additional resources for network management at the FPGA side.

The AXI4-Lite host interface permits control and configuration of the TCP IP core's registers and statistics for connection and link monitoring. The User application side and MAC connect to the TCP IP core with an easy to use AXI4-Stream interface. The TCP IP core can be configured to initiate (client) or accept (server) a TCP connection with a remote endpoint.

Once a session is established, data can be reliably sent and received over the TCP protocol; taking care of checksum insertion/checking, sockets and flow control at high, sustained data rates of 10 or 25 Gbit/s.

The User interface provides flow control, and manages multiple connections. Multiple simultaneous connections are supported, limited only by available packet buffer resources. Opening and closing connections is handled by the TCP core, with no requirement for additional software support. Re-transmit is handled by a control layer within the TCP for fast, easy error recovery.

Statistics are collected for all sent and received frames for traffic and connection analysis.



Chevin Technology IP Cores

UDP/IP Offload Engine

TCP/IP Offload Engine

10 & 25G Ethernet MAC

10 & 25G Ethernet PCS/PMA

10 & 25G LL MAC & PCS/PMA

ICMP/ARP – 10&25G support library

UDT4 – 10&25G UDT4 Server

6Gbit/s SSD Host Ctrl SATAv3.2

Markets

- Defence
- Scientific
- Aerospace
- Cybersecurity
- Medical
- Finance
- Telecoms
- Broadcast
- Data Centre

Applications

- Artificial Intelligence
- Machine Learning
- Video Imaging
- Image/Signal Processing
- Internet Security Monitoring
- Data Storage & Capture Systems
- Trade Execution & monitoring
- HPC/ Big Data systems
- Data Mining

10G Ethernet © 25G Ethernet © SSD STORAGE ©

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