

# Ultra Low-Latency 10Gbit/s Ethernet PCS

CT1010-XGPCS - Product Brief - Version 1.8 – 5th April 2019



The Chevin Technology XGPCS is an IP block which simplifies the FPGA integration of Ultra low-latency 10Gbit/s Ethernet connectivity in Xilinx FPGAs. Ultra-low latency is achieved by using only the PMA function in FPGA Multi-Gigabit transceivers and moving all PCS functions to code that is optimized for 10GBASE-R. This allows the data to take the shortest, and hence the lowest latency, path to and from the wire. The XGPCS is a PCS/PMA block that can be used directly with Multi-Gigabit Transceivers (SerDes & CDR logic) in any 10Gbit/s capable FPGA for the lowest possible latency. The application side can be driven by any XGMII compatible MAC with a 64bit interface at 156.25MHz. The PCS manages link encoding and scrambling, while adapting the data rate to the reference clocks. A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for frames, BER events, illegal codes and decode errors, which can be monitored through the Host Interface. Achieve smoother, faster integration with the Chevin Technology reference design on an AlphaData boards; ADMPCIE KU3, ADM-PCIE-8V3, ADM-PCIE-9V3, or a Xilinx KC705 development board, and a simple “ping” command line with the ICMP/ARP options. Use standard software TCP/UDP tools when integrated with

Chevin Technology’s XGTCP and XGUDP IP cores.

## Key Features

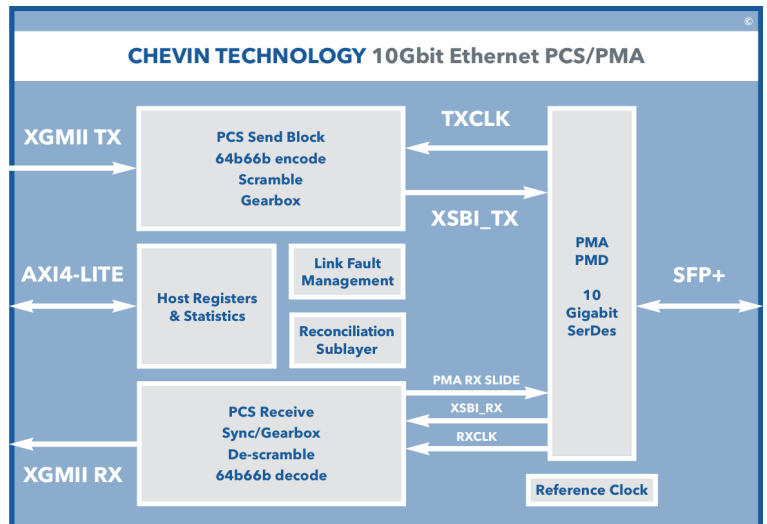
- Designed to IEEE 802.3ae-2002
- Low Latency PCS/PMA (RTT) 109 ns
- Small Footprint 2404 LUTs
- Integrated 64b66b encoder/decoder
- Integrated Scrambler/Descrambler
- Gearbox for rate conversion
- Fault management, BER monitoring
- Clock Rate adaptation, TX/ RX
- Detailed traffic analysis statistics collection
- XGMII interface, 64bit @ 156.25MHz
- XSBI interface, 32bit @ 322.265625MHz

## Latency Figures

First byte XGMII to XSBI output	38.1ns
First byte XSBI to XGMII output	32.4ns
Round trip delay, PCS only XGMII -> XSBI -> XGMII	70.5ns
Round trip delay, PCS/PMA XGMII -> SFP+ (wire) -> XGMII	109ns

## FPGA Resource Figures

Device: Kintex Ultrascale xcku060 -2  
PCS/PMA 2404 LUTs



## Deliverables

- Encrypted RTL/VHDL source code for simulation
- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Designs for Alpha-Data boards  
ADM-PCIE-KU3, ADM-PCIE-8V3, ADM-PCIE-9V3
- Simulation Test bench
- Build scripts for Vivado/ISE
- Support for integration into FPGA



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# 10Gbit/s Ethernet PCS XGPCS - Integration in FPGA

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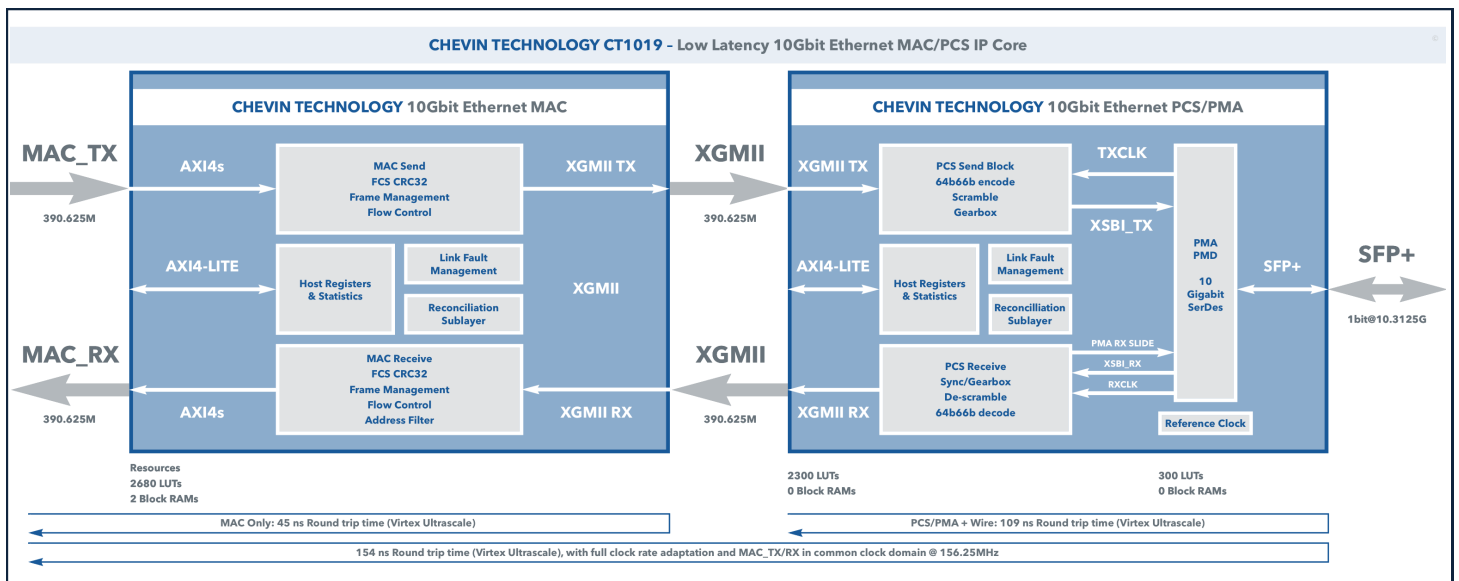


A simple host interface allows control and configuration of the XGPCS registers and statistics block. The reference design includes a simple host interface port and example host software to drive this interface, which can be used to speed up integration work.

The 32bit XSBI interface connects directly to any XSBI compatible PMA preferably utilizing Xilinx 7-series or Ultrascale devices' 10Gbit capable SerDes (Multi Gigabit Transceivers) with all the PCS functions bypassed which provides the lowest latency performance. Reference clock: 156.25MHz or 322.265MHz.

The application side connects directly to any XGMII compatible MAC.

We recommend pairing the XGPCS with Chevin Technology's XGMAC, an ultra-low-latency Ethernet MAC and other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.



## Chevin Technology IP Cores

- UDP/IP Offload Engine
- TCP/IP Offload Engine
- 10 & 25G Ethernet MAC
- 10 & 25G Ethernet PCS/PMA
- 10 & 25G LL Ethernet MAC & PCS/PMA
- ICMP/ARP—10&25G Support Library
- UDT4– 10 & 25G UDT4 Server
- 6Gbit/s SSD Host Ctrl SATA v 3.2

### Markets

- Defence
- Scientific
- Aerospace
- Cybersecurity
- Medical
- Finance
- Telecoms
- Broadcast
- Data Centre

### Applications

- Artificial Intelligence
- Machine Learning
- Video Imaging
- Image/Signal Processing
- Internet Security Monitoring
- Data Storage & Capture Systems
- Trade Execution & Monitoring
- HPC/Big Data Systems
- Data Mining



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