

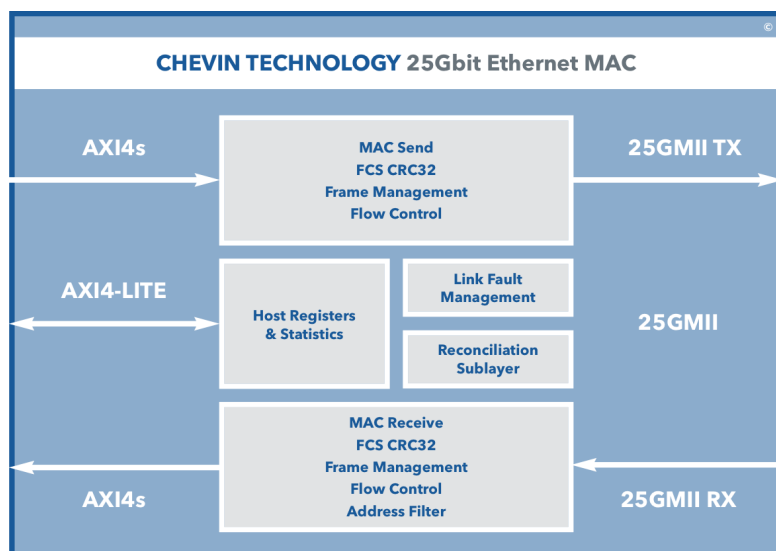
# Ultra Low-Latency 25Gbit/s Ethernet MAC



CT1025-25GMAC - Product Brief - Version 1.2 – 9th April 2019

The Chevin Technology 25GMAC IP core provides Ultra Low-Latency 25Gbit/s Ethernet connectivity in Xilinx Virtex® UltraScale™ FPGAs. The 25GMAC can be integrated into customers' products with an external or internal PCS, however we recommend using Chevin Technology's 25GPCS for simplified integration and lowest possible latency. The application side of the 25GMAC can be driven by any logic that generates and decodes Ethernet frames. The MAC manages frame timing, CRC32 Checksum insertion and generation, and manages the lower layer fault handling and 25GMII interface coding. Flow control provides back pressure to peer node and is handled automatically by the MAC in both directions independently. A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for different frame sizes, types and checksum errors. Achieve smoother, faster integration with the Chevin Technology reference design on an AlphaData boards; ADM-PCIE-8V3, ADM-PCIE-9V3, Xilinx Virtex® UltraScale™ and UltraScale+™ development boards. Use standard software TCP/UDP tools when integrated with Chevin Technology's XGTCP or XGUDP IP cores.

## Key Features



- Designed to IEEE 802.3-2008 Specification
- Low Latency 20.5 ns
- Integrated FCS CRC32 check/generate
- Small Footprint, 2680 LUTs
- Flow Control option with Pause packets
- Programmable max frame length
- Reconciliation Layer -Local /Remote Faults
- Programmable Inter Frame Gap
- Deficit Idle Count for maximum throughput
- Cut-through mode for lowest latency
- Store-and-forward for minimum app load
- MAC address filtering options
- Detailed traffic analysis statistics collection

## Latency Figures

First byte App IF to first byte 25GMII	<b>12.8ns</b>
First byte 25GMII to first byte App IF	<b>7.7ns</b>
Full Round trip time, including MAC/PCS/PMA AppTX -> SFP+ (wire) -> AppRX	<b>119.5 ns</b>

## FPGA Resource Figures

25GMAC - Cut-through	<b>2680 LUTs</b>
Options: Store & Forward	<b>4 BRAMs</b>

## Deliverables

- Encrypted compiled netlist
- Datasheet & User Guide
- Reference Designs
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA



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# 25Gbit/s Ethernet MAC

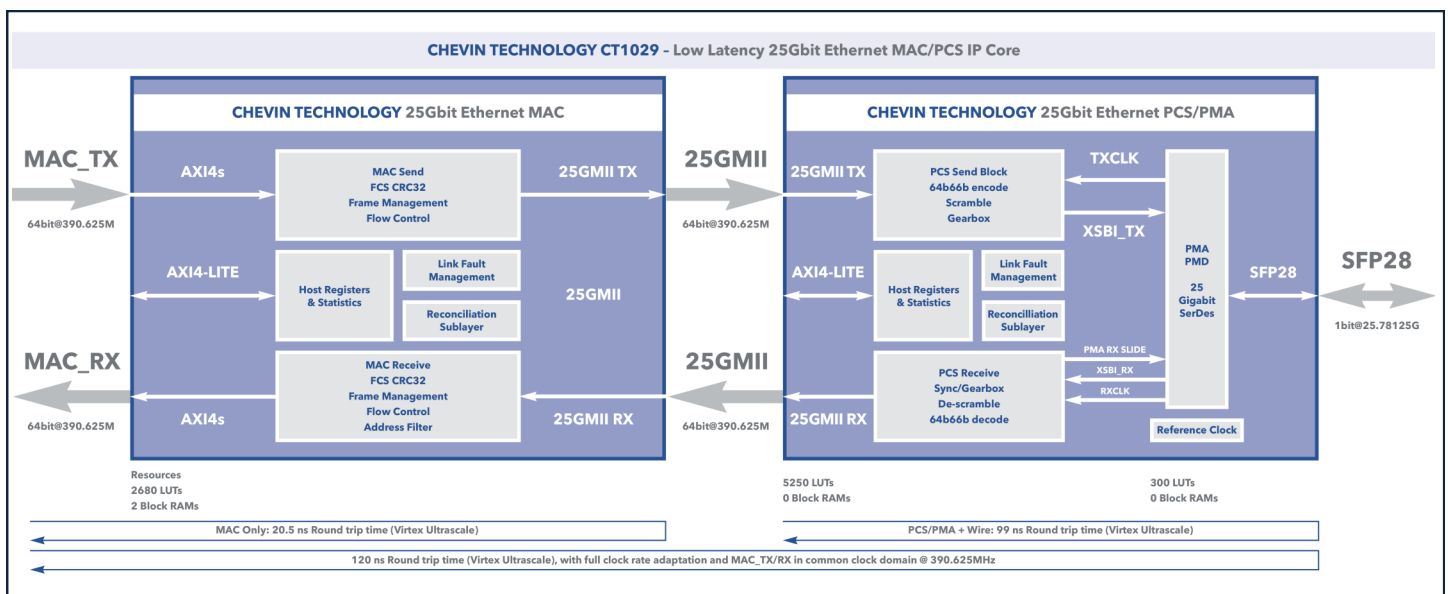
## 25GMAC - Integration in FPGA

Integration is made simple using the reference design, which includes the PCS function and a block for UDP/ICMP/ARP.

The UDP based host interface allows control and configuration of the 25GMAC registers and statistics block. The reference design documentation describes how to add constraints and build the MAC block into your application.

The 64bit 25GMII interface connects directly to any 25GMII compatible PHY, preferably utilizing Virtex® UltraScale™ devices that are 25Gbit capable. This combination provides the lowest possible latency, power, board size and cost, and the best overall performance.

We recommend pairing the 25GMAC with Chevin Technology's 25GPCS, an ultra-low-latency 25GBASE-R block for SFP28 DA copper cable or Fiber connection. The application side connects directly to user logic which can be user logic FIFOs to AXI4 standard interfaces, or shared via an arbiter to other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.



## Chevin Technology IP Cores

- UDP/IP Offload Engine
- TCP/IP Offload Engine
- 10 & 25G Ethernet MAC
- 10 & 25G Ethernet PCS/PMA
- 10 & 25G LL MAC & PCS/PMA
- ICMP/ARP – 10&25G support library
- UDT4 – 10&25G UDT4 Server
- 6Gbit/s SSD Host Ctrl SATAv3.2

### Markets

- Defence
- Scientific
- Aerospace
- Cybersecurity
- Medical
- Finance
- Telecoms
- Broadcast
- Data Centre

### Applications

- Artificial Intelligence
- Machine Learning
- Video Imaging
- Image/Signal Processing
- Internet Security Monitoring
- Data Storage & Capture Systems
- Trade Execution & Monitoring
- HPC/Big Data systems
- Data Mining



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