



SSD SATA 3.0 Host Controller 1.5/3/6Gbit/s for Xilinx FPGA

CT1202-SATA-HC - Product Brief - Version 1.2 – 22 Mar 2016

Introduction

The Chevin Technology SATA-HC IP block simplifies the integration of high capacity SSDs with FPGAs utilizing SATA I/II/III at 1.5/3/6Gbit/s data rates using Xilinx FPGAs.

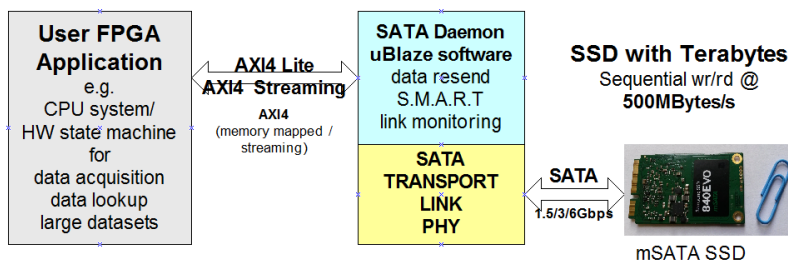
Combined low-latency and high throughput is achieved by accessing the SSD directly from FPGA logic with no external circuitry. The lower protocol layers Phy/Link/Transport are implemented in an all-RTL solution, which minimizes access time by providing the shortest possible path between SSD and application.

Paired with an SSD such as Samsung 850EVO the SATA-HC can provide Terabytes of non-volatile memory in a small, lightweight, low-power and cost effective package. Data access times are dominated by the SSD drive in use ranging from only a few microseconds for cached data or a few milliseconds for non-cached data.

The SATA-HC is ideally paired with an Application layer to support some or all ATA commands as required. Chevin Technology provides embedded solutions for the Application layer that utilise the Microblaze processor and software to support higher protocol layer functions such as data payload FIS re-send/receive on error.

The SATA-HC can also be run without an operating system OS/AHCI completely stand-alone for the absolute minimum latency, power, complexity and logic footprint.

Chevin Technology SATA Host Controller
providing access to Terabytes of fast non-volatile memory



Key Features

- Designed to SATA v3.0 (6Gbps)
- Low Latency, SATA commands <1us
- High Throughput read/write @ 500MByte/s
- Small Footprint 3042 LUTs (lower layers)
- PHY/LINK/Trans/App layers in RTL
- DMA management SW in embedded CPU
- Host operating system not required
- S.M.A.R.T data collection
- Fault management, BER monitoring
- Detailed traffic analysis & statistics collection
- Client Interface, 32bit write/read streaming @ 37.5/75/150MHz (1.5/3/6 Gbps)

“Drop the SATA-HC IP Block into your FPGA design for Low-latency connectivity to vast amounts of storage for your application”

Markets

- Data Centre
- Telecoms
- Finance
- Broadcast
- Defense/ Government
- Oil and Gas
- Test & Measurement

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining

Phone: +44 1943 601 700

Email: ip@chevintechnology.com

www.chevintechnology.com/technology/ct1202-sata

Chevin Technology SATA-HC

Integration in FPGA

The SATA-HC reference design provides a fast and easy integration path to include SSD connectivity in a Xilinx FPGA and does not require detailed knowledge about Gigabit transceivers or the SATA protocol.

The SATA-HC can be used directly with any Xilinx Ultrascale & 7-series Kintex/ Virtex up to 6Gbps and Spartan6 LXT up to 3Gbps.

A 150MHz reference clock supports SATA serial links at the three serial rates of 1.5, 3 and 6Gbps, while the logic and data path runs at 37.5, 75 & 150MHz internally on a 32bit wide data path. Data to/from a connected SATA device is made simple through the use of a streaming interface.

The register and control interface provides access SATA-HC registers and statistics block for monitoring low level parameters such as Phy CDR lock & raw BER, Link CRC32 and Transport layer FIS retries.

The SATA-HC connects to an application that can issue ATA commands.

A reference design for the AlphaData ADM-KU3 board shows how the SSD's sectors can be accessed using the LBA48 protocol, providing up to 144Petabytes of usable address space. The example also reports information such as installed SSD size, serial number, drive capabilities, S.M.A.R.T statistics for total hours count, power-on cycles, percentage lifetime used, CRC32 failures seen at the SSD side. Depending on the installed SSD, the SATA-HC can also perform secure wipe and other advanced functions.

Deliverables

- Encrypted RTL/VHDL source code
- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Design on Alpha Data ADM KU3 FPGA board
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA

Throughput Figures

The SATA-HC provides consistently high sustained throughput.

Example with Samsung EVO850 mSATA

3Gbps (Ultrascale & 7-series, Spartan6LXT)
Sequential write/read **270 MByte/s**

6Gbps (Ultrascale & 7-series Kintex/Virtex)
Sequential write/read **500 MByte/s**

Latency Figures

The SATA-HC provides consistently low and predictable latency, along with fast locking for hot plugging applications. Latency is largely dominated by the SSD response time as shown.

SSD: byte out from un-cached area **1800 us**
SSD: byte out from cached area **30 us**

FPGA: 1st byte in to DMA request sent **1 us**

FPGA Resource Figures

SATA Core (Trans/Link/Phy/GTH)

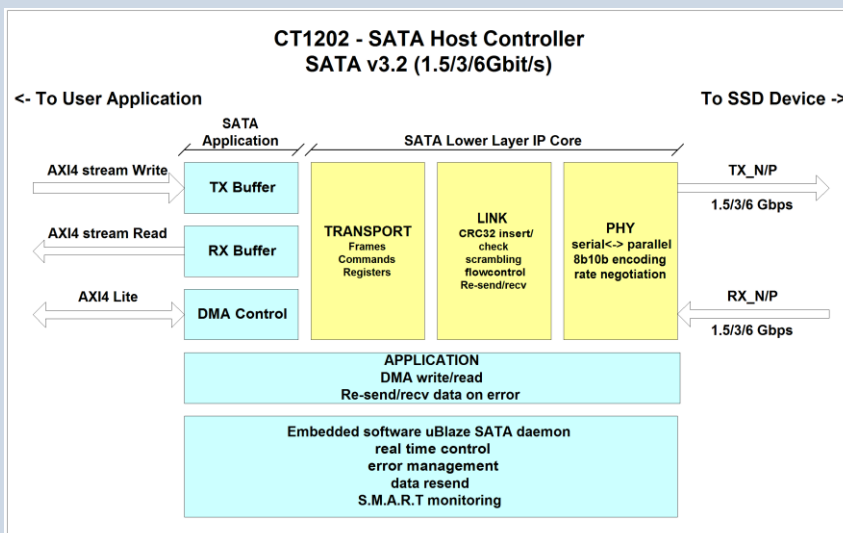
Gigabit Transceivers GTX /GTH, the PMA adaptation layer, is included in the gate count.

ADMKU3 Kintex Ultrascale **3042 LUTs**

KC705 Kintex7 **3150 LUTs**

Other Chevin Technology IP

- XGMAC 10Gbit/s Ethernet MAC
- XGPHY 10Gbit/s Ethernet PHY
- XGTCP 10Gbit/s TCP Server/Client
- XGUDP 10Gbit/s UDP Server/Client.
- XGICMP/ARP 10Gbit/s support library
- XGUDT4 10Gbit/s UDT4 Server



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